Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An apparatus having a CPU wherein the improvement comprises:

a clock generator generating a first clock signal for the CPU, and a second clock for the bridge controller, wherein the first and second clock signals are two distinct clock signals outputted by the clock generator and have different frequencies; and

a bridge controller comprising a logic device for ~~adjusting~~ outputting the second clock signal adjusted based on a power source and independent of the first clock signal.

2. (Currently Amended) The apparatus of claim 1, wherein the bridge controller controls a clock speed of a bus connected between the CPU and the bridge controller for data communication among a plurality of peripheral devices of the apparatus using the adjusted second clock.

3. (Previously Presented) The apparatus of claim 1, wherein the power source is one of AC power mode and battery power mode.

4. (Canceled)

5. (Previously Presented) The apparatus of claim 1, wherein the apparatus further includes a video processor and the clock generator generates a third clock signal for the video processor, the third clock signal being distinct from the first and second clock signals and having a different frequency than the first and second clock signals.

6. (Previously Presented) The apparatus of claim 5, wherein the improvement further comprises a second logic device for receiving the third clock signal and adjusting the third clock signal based on the power source.

7. (Previously Presented) The apparatus of claim 5, wherein the first clock signal has a higher frequency than the second clock signal and the second clock signal has

a higher frequency than the third clock signal, and wherein the bridge controller controls a clock speed of a bus for data communication with the CPU.

8. (Previously Presented) The apparatus of claim 1, wherein the logic device increases a frequency of the second clock signal in an AC power mode and outputs the second clock signal without a frequency adjustment in a battery power mode.

9. (Previously Presented) The apparatus of claim 1, wherein the logic device outputs the second clock signal in a battery power mode without a frequency adjustment.

10. (Previously Presented) The apparatus of claim 6, wherein the second logic device increases a frequency of the third clock signal in an AC power mode and outputs the third clock signal without a frequency adjustment in a battery power mode.

11. (Previously Present) The apparatus of claim 6, wherein the second logic device outputs the third clock signal in a battery power mode without a frequency adjustment.

12. (Currently Amended) An apparatus having a CPU and a bridge controller, wherein the improvement comprises:

a clock generator generating a first clock signal; and

a clock adjustor receiving the first clock signal and operating in a power source mode, said clock adjustor generating a second clock signal for the CPU and a third clock signal for the bridge controller, wherein the second and third clock signals are two distinct clock signals outputted by the clock adjustor and have frequencies that are independent of each other, wherein the apparatus further includes a video processor and the clock adjustor generates a fourth clock signal for the video processor, the fourth clock signal being distinct from the second and third clock signals and having a different frequency than the second and third clock signals.

13. (Previously Presented) The apparatus of claim 12, wherein the bridge controller controls a clock speed of a bus for data communication among a plurality of peripheral devices of the apparatus.

14. (Currently Amended) The apparatus of claim ~~12~~ 13, wherein the clock adjustor is a phase locked loop (PLL), and wherein the bus is a host bus.

15. (Previously Presented) The apparatus of claim 12, wherein the CPU further comprises a phase locked loop (PLL) receiving the second clock signal for the CPU and adjusting the second clock signal based on one of AC power mode and battery power mode.

16. (Cancelled)

17. (Currently Amended) The apparatus of claim ~~16~~ 12, wherein the second clock signal has a higher frequency than the third clock signal and the third clock signal has a higher frequency than the fourth clock signal.

18. (Previously Presented) The apparatus of claim 12, wherein the power source is one of an AC power mode or a battery power mode.

19. (Currently Amended) A method for performing clock speed generation, comprising:

receiving a base clock signal;

selectively multiplying the base clock signal by a first factor to produce a first higher frequency clock signal, and by a second factor to produce a second higher frequency clock signal, wherein the first and second higher frequency clock signals are different and phase-locked with the base clock signal;

receiving a power mode signal; ~~and~~

selectively outputting the first higher frequency clock signal to a first device and the second higher frequency clock signal to a second device based on the power mode signal, wherein the first device is a processor and the second device is a bridge controller; and

generating a third higher frequency clock signal for a video processor, wherein the third clock signal being distinct from the first and second clock signals and having a different frequency than the first and second clock signals.

20. (Previously Presented) The method of claim 19, wherein the power mode signal is an AC power mode signal or a battery power mode signal and the second higher frequency clock signal is selectively output independent of the first higher frequency clock signal.

21. (Currently Amended) A method for performing clock speed generation, comprising:

supplying a first clock signal by a first logic to generate a first higher frequency clock signal to a CPU;

supplying a second clock signal by a second logic to generate a second higher frequency clock signal to a bridge controller, wherein the first and second clock signals are distinct;

receiving by the second logic, a power mode signal and adjusting the second clock signal; and

selectively outputting the second higher frequency clock signal based on the power mode signal independent of the first clock signal, wherein the bridge controller controls a clock speed of a bus connected therebetween for data communication with the CPU using the outputted second higher frequency clock signal.

22. (Currently Amended) The method of claim 21, wherein the first clock signal is greater than the second clock signal, wherein ~~a bridge controller controls a clock speed of a bus for data communication with the CPU, and wherein~~ the power mode signal is an AC power mode signal or battery power mode signal.

23. (Previously Presented) The method of claim 21, wherein the first logic and the second logic are PLLs (Phase Locked Loop).

24. (Cancelled)

25. (Previously Presented) The apparatus of claims 6, wherein the first logic is a phase locked loop (PLL) and the second logic device is a PLL.

26. (Previously Presented) The apparatus of claim 12, wherein the clock adjuster adjusts the third clock signal for the bridge controller based on the power source mode and independent of the second clock signal.

27. (Previously Presented) The apparatus of claim 12, wherein the second and third clock signals are independent of each other in each of at least two power source modes, and wherein the second clock signal includes at least two different frequencies selected in accordance with the power source mode.

28. (Previously Presented) The method of claim 19, wherein the second higher frequency clock signal is selectively output independent of the first higher frequency clock signal, and wherein the second higher frequency clock signal is selectively output by being output as is or reduced according to the power mode signal.

29. (Cancelled)

30. (Previously Presented) The method of claim 19, wherein the second higher frequency clock signal has at least two different frequencies selected in accordance with the power mode signal.